2112

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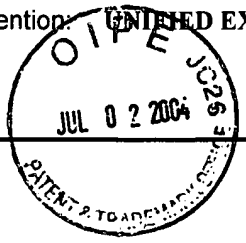
CERTIFICATE OF MAILING BY FIRST CLASS MAIL (37 CFR 1.8) Applicant(s): **Brenner et al**			Docket No. **2000.021/1109.005**
Serial No. **09/736,567**	Filing Date **12/13/2000**	Examiner **Knoll, Clifford H**	Group Art Unit **2112**

Invention: **UNIFIED EXCEPTION HANDLING FOR HIERARCHICAL MULTI-INTERRUPT ARCHITECTURES**



I hereby certify that this **Amendment Transmittal Letter; Response & Amendment; Acknowledgement Postcard**
(Identify type of correspondence)

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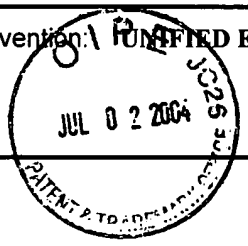
P07A/REV03

AMENDMENT TRANSMITTAL LETTER (Large Entity) Applicant(s): **Brenner et al**	Docket No. **2000.021/1109.005**

Serial No.	Filing Date	Examiner	Group Art Unit
09/736,567	12/13/2000	Knoll, Clifford H	2112

Invention: **UNIFIED EXCEPTION HANDLING FOR HIERARCHICAL MULTI-INTERRUPT ARCHITECTURES**



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TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated and is transmitted as shown below.

CLAIMS AS AMENDED

	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST # PREV. PAID FOR		NUMBER EXTRA CLAIMS PRESENT	RATE	ADDITIONAL FEE
TOTAL CLAIMS	28	-	32	=	0	x $18.00	$0.00
INDEP. CLAIMS	8	-	12	=	0	x $86.00	$0.00
Multiple Dependent Claims (check if applicable) ☐							$0.00
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT							$0.00

☒ No additional fee is required for amendment.

☐ Please charge Deposit Account No. _____ in the amount of _____

☐ A check in the amount of _____ to cover the filing fee is enclosed.

☒ The Director is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. **50-0734**

- ☒ Any additional filing fees required under 37 C.F.R. 1.16.
- ☐ Any patent application processing fees under 37 CFR 1.17.

Signature

Dated: 6/30/04

Richard L. Sampson, Reg. 37,231
Sampson & Associates, P.C.
50 Congress Street
Boston, MA 02109

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25779
PATENT TRADEMARK OFFICE

CC:

P11LARGE/REV06

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Brenner et al

Serial No.: 09/736,567 Group Art Unit: 2112

Filed: 12/13/2000 Examiner: Knoll, Clifford H

Title: Unified Exception Handling For Hierarchical Multi-Interrupt Architectures

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on June 30, 2004.

Richard L. Sampson, Jr.
Attorney for Applicants
Reg. No. 37,231

Date of Signature: June 30, 2004

To: Commissioner For Patents
Mail Stop Amendment
Alexandria, VA 22313-1450

RESPONSE AND AMENDMENT UNDER 37 CFR §1.121

Dear Sir:

This paper is filed in response to the second Office Action mailed 04/06/2004 (PTO Prosecution File Wrapper Paper No. 7). A response is due by July 6, 2004. This response is being filed on or before 07/06/2004, therefore, this response is being timely filed.

Amendments

Please amend the above-identified U.S. application as follows:

In The Specification

Please amend the portions of the specification as indicated by the following marked up versions thereof:

Please substitute the full paragraph beginning on line 11 of page 13 with the following:

This embodiment of the present invention makes use of specific architecture features to merge the two interrupt streams into a single handler, while unambiguously identifying the source of each interrupt. Turning now to Fig. 2, this embodiment of the present invention includes a single instruction referred to as a Move Status Register (MSR) instruction 20. This instruction 20 serves to simultaneously disable both FIQs and IRQs upon receipt of an IRQ exception. This instruction 20 is inserted at IRQ vector address 12. Thus, upon receipt of an IRQ, i.e., when the PC branches to IRQ vector 12, the MSR~~MRS~~ instruction 20 disables any subsequent interrupts (both IRQ and FIQ). Instruction 20 accomplishes this by inserting an F bit in the Current Processor Status Register (CPSR) to disable FIQs, and by leaving the I bit set (the I bit is automatically set upon a branch to the IRQ vector 12) or re-setting the I bit.

Please substitute the full paragraph beginning on line 21 of page 14 with the following:

As mentioned hereinabove, the ARM® architecture sets mode bits within the CPSR that correspond to the type of exception, i.e., either IRQ or FIQ. The architecture also ensures that the first instruction at the vector table is executed without interruption. This embodiment utilizes this latter feature to effectively ensure that the inserted MSR~~MRS~~ instruction 20 is properly executed.